REMARKS

Claims 17-25 are presented for examination. Claim 17 has been amended, and claims 21-25 are new.

In the Office Action mailed May 31, 2002, the Examiner rejected claims 17, 19, and 20 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 4,811,065 ("Cogan"). Claim 18 was rejected under 35 U.S.C. § 103(a) as unpatentable over Cogan in view of European Patent 0747969A1 ("Pearce"). Applicant respectfully disagrees with the basis for the rejections.

Turning to the claims, claim 17 is directed to a method of operating a vertical DMOS transistor in an integrated circuit. Cogan does not teach or suggest operating a vertical DMOS transistor in an integrated circuit. The vertical DMOS transistor has a Schottky diode formed by a metallic source contact coupled to the source and to the epitaxial layer. The transistor also includes a body formed of second conductivity in the epitaxial layer to form a pn junction diode with a drain of first conductivity formed in an epitaxial layer of the same conductivity. The method of operating includes diverting current from the body-to-drain pn junction using the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor.

In Cogan, U.S. Patent No. 4,811,065, a conventional vertical DMOS transistor having a Schottky diode placed in parallel with the body diode is disclosed. The Schottky diode is forward biased by a voltage drop that is lower than the voltage drop needed to forward bias the body diode. As such, the Schottky diode bypasses all current from the source of the DMOS transistor while preventing the body diode from becoming forward biased. While this structure increases the operational speed of the DMOS transistor by reducing the storage of minority carriers in the body diode, this does not account for the effects of parasitic BJT's associated with a power DMOS structure on an integrated circuit having many other transistors on the same substrate. In view of the foregoing, applicant respectfully submits that claim 17 is clearly in condition for allowance, as are dependent claims 18-20.

New claims 21-25 are a method of operating a vertical DMOS transistor in an integrated circuit with the DMOS transistor having the structure as set forth in the independent claims of the parent case, U.S. Patent No. 5,925,910. More particularly, the structure of independent claims 1, 6, 7, and 9 a combination of claims 9-11 and 9-12 are found in new claims

21-25. Inasmuch as these method of operating claims are based on the structure that has previously been allowed over the Cogan reference, applicant respectfully submits that new claims 21-25 are clearly allowable.

In view of the foregoing, applicant submits that all of the claims in this application are in condition for allowance. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version With Markings to Show Changes Made."**

Respectfully submitted,

Paolo Menegoli

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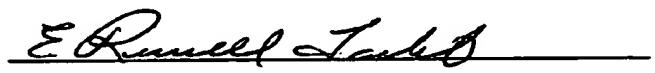

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 21-25 have been added.

Claim 17 has been amended as follows:

17. (Twice Amended) A method of operating a vertical DMOS transistor in an integrated circuit, the transistor having a drain of first conductivity formed in ~~an expitaxial layer~~ a buried region of same conductivity, a body formed of second conductivity in ~~the~~ an epitaxial layer of first conductivity to form a pn junction diode with the drain, a source of first conductivity in the body, a gate electrode positioned above the source, the body, and the epitaxial layer, a conductive contact coupled to the drain, and a metallic source contact coupled to the source and to the epitaxial layer to form a Schottky diode, comprising diverting current from the ~~source~~ body-to-drain pn junction of the DMOS transistor with the Schottky diode that is co-integrated with the DMOS transistor when the source becomes more positive than a drain of the DMOS transistor and the gate has not induced a channel region between the source region and the drain region.

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